ASYNCHRONOUS DATA BUFFER AND A METHOD OF USE THEREOF

FIELD OF THE INVENTION

The present invention relates generally to network data transfer systems and specifically to an asynchronous data buffer and a method of use thereof.

BACKGROUND OF THE INVENTION

Many conventional network data transfer systems utilize cell relay systems to transfer data. The objective of cell relay systems is to develop a single high-speed network based on a switching and multiplexing scheme that works for all data types. Cell relay is a generic term for a packet switching protocol using fixed length packets or cells. A packet or cell is a bundle of data, usually in binary form, organized in a specific way for transmission.

A network data transfer system ordinarily involves a sending device and a receiving device. However, because the sending device usually has a different data rate/flow than the receiving device, data buffers typically are utilized. A buffer is a temporary storage location for information being sent or received and is located between two different devices that have different rates for handling the data. Figure 1 is an example of a typical data transfer environment. This environment includes a sending device 10, a buffer 12, and a receiving device 14. The buffer 12 includes a write element 11 for writing data cells into the buffer 12 from the sending device 10 and a read element 13 for reading data cells from the buffer 12 to the receiving device 14. Basically, the buffer acts like a dam. It captures the data cells from the sending device 10 and then sends them out at a rate that can be handled by the receiving device 14.

However, conventional systems require that each data cell being transferred be

completely written into the buffer 12 before it can be read out. A problem with this type of implementation is the latency involved during data transfer. Latency is the time elapsed from when the data cell first enters the system to when the data cell begins to leave the system. Another problem with the conventional implementation is the larger amount of buffer space needed to prevent over and under runs.

Accordingly, what is needed is a smaller data buffer that reduces latency during data transfer. The present invention addresses such a need.

SUMMARY OF THE INVENTION

A data buffer in accordance with the present invention is disclosed. The data buffer comprises an entry section and a signaling circuit coupled to the entry section, the signaling circuit for signaling the data buffer to transfer a portion of a data cell from the entry section prior to the data cell being completely received by the entry section.

Through the use of the data buffer in accordance with the present invention, data transfer systems are improved in two ways. First, by enabling data to be transferred before it is completely stored into the buffer, the latency that is typically required for data cell transfer is reduced. Second, the buffer storage space that is typically required to store a complete data cell is also reduced. This two-fold improvement produces increased data transfer rates while decreasing the amount of required buffer storage space.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an example of a typical data transfer environment.

Figure 2 is a high level flowchart of the method of the present invention.

Figure 3 shows a data buffer in accordance with the present invention.

Figure 4 is a flowchart of the operation of the data buffer in accordance with the preferred embodiment of the present invention.

DETAILED DESCRIPTION

The present invention discloses a data buffer. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

To more particularly describe the method accordance with the present invention, Figure 2 is a simple flowchart of a method in accordance with the present invention. First, data from a data cell is allowed to be written into the data buffer, via step 50. Next, the data cell is read from the data buffer prior to the data cell being completely written into the data buffer, via step 52.

The present invention is presented in the context of a preferred embodiment. The preferred embodiment of the present invention provides an improved asynchronous data buffer. Through the use of the data buffer in accordance with the present invention, data cell transfer latency is reduced. Furthermore, the amount of required buffer storage space is decreased since the buffer storage space that is typically required to store a complete data cell is reduced.

The asynchronous data buffer in accordance with the present invention operates on the premise that programmable data transfer threshold settings can be established in order to allow a data cell to begin being read out of the data buffer prior to the entire data cell being written into the data buffer. Furthermore, the data buffer in accordance with the present invention allows another cell to be written in even if the current cell is not completely read. Preferably, these threshold settings are determined based on mathematical algorithms or empirical data related to the data transfer process. However, one of ordinary skill in the art will readily recognize that a variety of methods could be used to determine the threshold settings while remaining within the spirit and scope of the present invention.

As previously shown, a buffer comprises a write element and a read element. Accordingly, the threshold settings are derived based on the knowledge that at a certain point during the data transfer process, the read element can't possibly get ahead of the write element, even if it is running faster. The reverse is true for the write element. After a certain amount of the data cell has been read out of the data buffer, this amount being less than the full amount, the write element can begin writing a subsequent data cell into the buffer with no danger of data corruption.

It should also be noted that the asynchronous operation of the data buffer in accordance with the present invention is not simply limited to equal but out of phase frequencies. The asynchronous data buffer in accordance with the present invention can operate with two distinctly different frequencies. For example, the write side may run at 10ns, while the read side may run at 8ns. The decoupling of the read and write sides, along with the communication between the two sides via the asynchronous signaling circuitry allows for this type of flexibility when the threshold settings are properly tuned.

In order to facilitate the method in accordance with the present invention, a read-signal is provided to the data buffer once the data cell being transferred has reached the threshold setting (i.e. before the entire data cell is written into the buffer). Once the read-signal is provided, the data buffer begins reading the partially written data cell out of the data buffer. In addition, as the data cell is being read out of the buffer, a write-signal is provided to indicate that a subsequent data cell can begin being written into the data buffer. Although the write-signal is provided prior to the initial data cell being completely read from the data buffer, the threshold settings are established so that data corruption is avoided. Data being read out of the buffer can be corrupted if a subsequent data cell being written into the buffer "catches up" with the data being read out of the buffer and overwrites it.

To better understand the present invention, Figure 3 shows a data buffer in accordance with the present invention. The data buffer comprises a write element (writer) 100, a buffer entry section 150 and a read element (reader) 200. The writer 100 and the reader 200 comprise similar logic structures. The writer 100 and reader each comprise an entry pointer 102, 202 which indicates which data cell is currently being transferred; an item pointer 104, 204 which indicates which specific portion of the data cell is being transferred; and an entry counter 106, 206 which counts how many data cells have been processed (i.e., the write element's entry counter 106 indicates how many data cells have been written but not read and the read element's entry counter 206 indicates how many data cells are left).

The data buffer in accordance with the present invention also includes an asynchronous circuit 152. The asynchronous circuit 152 includes an "add" signaling portion 154 and a "remove" signaling portion 156 and is employed to allow the writer 100 and reader 200 to communicate with each other. Using conventional methodology, a reader is designed to read a

data cell from the buffer entry section only when the data cell has been completely written into the buffer entry section. However, by utilizing the data buffer in accordance with the present invention, data is transferred with a finer granularity.

What is meant by a finer granularity is that the data buffer in accordance with the present invention is programmed to transfer data cells at a byte-access level. What is meant by a byte- access level is that each of a plurality of portions of the data cell are written into the buffer entry section 150 via a byte-access to the buffer entry section 150. For example, 16 byte-accesses to the buffer entry section 150 are required for an entire data cell to be written into the buffer entry section 150. Accordingly, at a predetermined threshold point, i.e. at a point prior to the entire data cell being written into the buffer entry section 150, the reader can't possibly get ahead of the writer. At this predetermined threshold point, for example after the 8th byte-access, the asynchronous circuit 152 provides a signal to the reader 200 to begin reading the data cell.

Although the above outlined description discloses the utilization of a data cell requiring 16 accesses to the buffer entry section wherein the predetermined threshold point is after the 8^{th} access, one of ordinary skill in the art will readily recognize that the number of required access for a data cell and the respective predetermined threshold could vary while remaining within the spirit and scope of the present invention.

By transferring cells at a finer granular level (i.e. via byte-access as opposed to whole cell accesses), the asynchronous data buffer can overcome inefficiencies in the control logic of buffers downstream from it. For example, for cell transfers from chip to chip, there is an inherent latency in starting and stopping cell transfers. By generating thresholds on a byte-access level, the full and empty signals are more timely and can thus over come these

inefficiencies.

This same concept is also utilized with regard to the writer 100. At another predetermined threshold point prior to the entire data cell being read from the buffer entry section 150, the writer 100 can begin writing a subsequent data cell into the buffer entry section 150 with no danger of corrupting the data being read out of the buffer entry section 150.

To better understand the operation of the data buffer in accordance with the present invention, please refer to Figure 4. Figure 4 is a flowchart of the operation of the data buffer in accordance with the preferred embodiment of the present invention. The process begins with a number of data cells needing to be written into the buffer entry section. First, the writer begins to write the first data cell into the buffer entry section by accessing the buffer entry section, via step 300. Next, the writer's item pointer is incremented each time the writer accesses the buffer entry section to write the first data cell, via step 302. Once the item pointer reaches a predetermined threshold, the predetermined threshold being set at a point before the first data cell is completely written into the buffer entry section, the asynchronous signaling circuit signals the reader to increment its entry counter, via step 304. This is done via the "add" signaling portion. Preferably, before data is written into the buffer entry section, the reader's entry counter is zero. Accordingly, zero cells are available to be read. Once, the reader's entry counter is non-zero, this indicates that the buffer entry section is non-empty and the reader can begin reading data from the buffer entry section.

Next, the reader begins reading the first data cell from the buffer entry section by accessing the buffer entry section, via step 306. The reader's item pointer is then incremented each time the reader accesses the buffer entry section, via step 308. Once the reader's item

pointer reaches a predetermined threshold, the asynchronous signaling circuit signals the writer's entry counter to decrement, via step 310. Preferably, this is done via the "remove" signaling portion of the asynchronous circuit. The writer's entry counter is then decremented, thereby reducing by one the number of data cell entries written, but not read, into the buffer entry section, via step 312. The writer can now begin writing a second data cell entry into the buffer entry section once the first data cell is completely written into the buffer entry section. However, when the total buffers available to write have not been read, the system is characterized as full. Consequently, once the "removed" signal comes to the writer, the system is no longer full and the writer can begin writing another data cell into the buffer entry section.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.